(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : 0 519 741 A2

(12) # EUROPEAN PATENT APPLICATION

(21) Application number : 92305660.0

(51) Int. Cl.^{5} : H01L 29/06

(22) Date of filing : 19.06.92

(30) Priority : 21.06.91 JP 150576/91

(43) Date of publication of application : 23.12.92 Bulletin 92/52

(84) Designated Contracting States : CH DE IT LI

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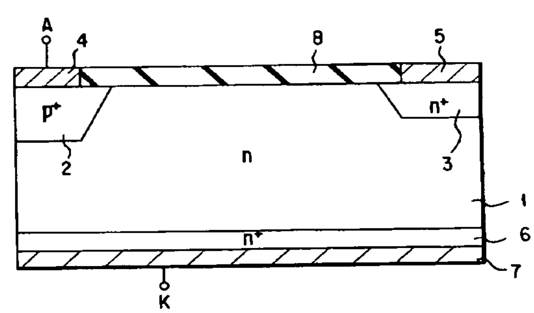
(54) **High-breakdown-voltage semiconductor element.**

(57) In a high-breakdown-voltage diode, a high-concentration p-type layer (2) is selectively formed in an n-type silicon layer (1), and a high-concentration n-type layer (3) is formed in the same separate from the layer (2) by a predetermined distance. An insulation film (8) having a dielectric constant larger than silicon is formed on that portion of the n-type silicon layer (1) which extends between the layers (2, 3), for relaxing concentration of an electric field caused in the surface of the substrate.



F I G. 1

EP 0 519 741 A2

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This invention relates to a high-breakdown-voltage semiconductor element.

A technique of providing a guard ring around an end pn-junction formed in an element region to be supplied with a high voltage is known as a method of increasing the breakdown voltage of a semiconductor element. The guard ring reduces the degree of electric field concentration at a tip portion of a depletion layer extending from the pn-junction, thereby increasing the breakdown voltage of the element. The effect of reducing the degree of the electric field concentration is obtained by optimally designing the depth of diffusion of the guard ring layer, the distance between the guard ring layer and a terminal region, and the distance between guard ring layers (if a plurality of guard ring layers are employed).

Fig. 16 shows an end portion of a high-breakdown-voltage diode having such a guard ring structure. A high-concentration p-type layer 2, which is to be an anode region, is formed in the upper surface of a high-resistance n-type silicon layer 1 (substrate). Further, a high-concentration n-type layer 3 is formed in the upper surface of the layer 1 separated from the layer 3 by a predetermined distance, for stopping the extension of a depletion layer. The layer 3 is provided with an electrode 5 for supplying a voltage identical to that of a cathode. High-concentration p-type layers 21 and 22 serving as guard rings are formed in the surface between the layers 2 and 3. An electrode 7 is formed on the lower surface of the layer 1 with a high-concentration n-type layer 6 interposed therebetween.

In such a structure, it is difficult to determine the distance between a guard ring layer and a terminal region, and the distance between guard ring layers in the case of employing a plurality of guard ring layers.

As described above, the conventional high-breakdown-voltage semiconductor element of a guard ring structure is hard to design.

This invention has been made in consideration of the above circumstances, and aims to provide a high-breakdown-voltage semiconductor element easy to design and having superior high-breakdown-voltage characteristics.

According to a first aspect of the invention, the high-breakdown-voltage semiconductor element has such a structure that a high-resistance semiconductor substrate of a first conductivity type has a second conductivity type layer of a high-concentration selectively formed therein and the first conductivity type layer of a high-concentration formed therein separated from the second conductivity type layer by a predetermined distance, the semiconductor element being characterized in that an insulation film having a dielectric constant larger than the semiconductor substrate is formed on the upper or lower surface of the high-resistance semiconductor substrate between the first and second conductivity type layers.

According to a second aspect of the invention, the high-breakdown-voltage semiconductor element is characterized by comprising first and second conductivity-type layers, first and second electrodes provided on the substrate such that they are located one on either side of a junction of the first and second conductivity-type layers, and an insulation film having a dielectric constant larger than the substrate and provided to connect the first and second electrode to each other.

As will be hereinafter explained in detail, the invention utilizes the characteristic that the state of an electric field caused in the insulation film depends upon conditions given thereto without being influenced by the ambient state, when the dielectric constant of the insulation film is sufficiently large. That is, where an insulation film having a dielectric constant larger than the substrate is provided on the outside of a pn-junction, such as an end one, in an element having a structure as in the invention, a uniform electric field is formed in the insulation film, so that electric field concentration in a region near the insulation film can be avoided when a high reverse bias voltage is applied to the element.

Thus, the invention can provide a high-breakdown-voltage semiconductor element employing an insulation film capable of reducing the degree of electric field concentration caused in that portion of the substrate which is located in the vicinity of the insulation film.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view, showing a high-breakdown-voltage diode according to a first embodiment of the invention;

Fig. 2 is a view, useful in explaining a reduction in the degree of concentration of an electric field by virtue of an insulating film having a large dielectric constant;

Fig. 3 is a cross sectional view, showing a high-breakdown -voltage diode according to a second embodiment of the invention;

Fig. 4 is a cross sectional view, showing a high-breakdown-voltage diode according to a third embodiment of the invention;

Fig. 5 is a cross sectional view, showing a high-breakdown-voltage diode according to a fourth embodiment of the invention;

Fig. 6 is a cross sectional view, showing a high-breakdown-voltage diode according to a fifth embodiment

of the invention;

Fig. 7 is a cross sectional view, showing a high-breakdown-voltage diode according to a sixth embodiment of the invention;

Fig. 8 is a cross sectional view, showing a high-breakdown-voltage diode according to a seventh embodiment of the invention;

Fig. 9 is a cross sectional view, showing a high-breakdown-voltage diode according to an eighth embodiment of the invention;

Fig. 10 is a cross sectional view, showing a high-breakdown-voltage diode according to a ninth embodiment of the invention;

Fig. 11 is a cross sectional view, showing a high-breakdown-voltage diode according to a tenth embodiment of the invention;

Fig. 12 is a cross sectional view, showing a high-breakdown-voltage diode according to an eleventh embodiment of the invention;

Fig. 13 is a cross sectional view, showing an IGBT (Insulated Gate Bipolar Transistor) according to a twelfth embodiment of the invention;

Figs. 14A-14G are cross sectional views, showing the manufacturing procedure of the IGBT shown in Fig. 13;

Fig. 15 is a cross sectional view, showing a thyrister according to a thirteenth embodiment of the invention; and

Fig. 16 is a cross sectional view, showing a conventional high-breakdown-voltage diode.

The embodiments of the invention will be explained with reference to the accompanying drawings.

Fig. 1 shows a high-breakdown-voltage diode according to a first embodiment of the invention. A high-concentration p-type layer 2 serving as an anode terminal is selectively formed in the surface of a high-resistance n-type silicon layer (substrate) 1, and a high-concentration n-type layer 3 for stopping the extension of a depletion layer is formed in the surface, separated from the layer 2 by a predetermined distance. An anode electrode 4 and an electrode 5 supply a voltage indentical to that of a cathode are formed on the layers 2 and 3, respectively. An insulation film 8 made of TiO_2 and having a dielectric constant larger than that of Si is formed on the upper surface of the n-type silicon layer 1 between the electrodes 4 and 5. A cathode electrode 7 is formed on the lower surface of the layer 1 with a high-concentration n-type layer 6 interposed therebetween.

When a reverse bias voltage is applied to the above high-breakdown-voltage diode between the anode and cathode electrodes 4 and 7, and between the electrodes 4 and 5, a depletion layer grows from the high-concentration p-type layer 2 into the n-type silicon layer 1. If the dielectric constant of the insulation film 8 is sufficiently larger than that of silicon, an electric field caused in the film 8 when the reverse bias voltage is applied is determined by the electrodes 4 and 5 irrespective of the ambient conditions. That is, the electric field is uniform in the horizontal direction, i.e., has a uniform potential gradient. As a result, the degree of concentration of the electric field is reduced in that portion of the silicon layer 1 which is located under the insulation film 8.

The effect of the insulation film 8 will be explained referring to Fig. 2. Fig. 2 shows a state in which a dielectric member A having a dielectric constant ε_1 is in contact with a dielectric member B having a dielectric constant ε_2. As regards a fine region Ω including the boundary surface between the dielectric members A and B, the following equation (1) can be obtained by using the Gauss' theorem:

$$\int_{\partial\Omega} \varepsilon E \cdot \vec{n} ds = Q \qquad \ldots (1)$$

$\vec{n}$; outward unit vector perpendicular to surface of region Ω

where Q represents the total charge accumulated in the region Ω. If the thickness d of the region Ω is sufficiently smaller than the length 1 of the region, the equation (1) can be replaced with the following equation (2):

$$\int_a^b \varepsilon_1 E \cdot \vec{n} dx + \int_b^a \varepsilon_2 E \cdot \vec{n} dx = \sigma \ell \qquad \ldots (2)$$

where ε_1 represents the dielectric constant of the portion of the region Ω_1 on the side of the dielectric member A, ε_2 the dielectric constant of the portion of the region Ω_2 on the side of the dielectric member B, and σ the density of charge accumulated in a line extending between a and b. The following equation (3) is obtained by dividing each side of the equation (2) by ε_2:

$$\frac{\varepsilon 1}{\varepsilon 2} \int_a^b E \cdot \vec{n} dx + \int_b^a E \cdot \vec{n} dx = \frac{\sigma \ell}{\varepsilon 2} \quad \ldots (3)$$

If ε_2 is sufficiently larger than ε_1 and than $\sigma\ell$, then the first term of the left side and the term of the right side will be very smaller than the second term of the left side. Thus, the following equation (4) can be obtained approximately:

$$\int_a^b E \cdot \vec{n} dx = 0 \quad \ldots (4)$$

From the equation (4), the following equation (5) is obtained

$$\frac{\partial \psi}{\partial n} = 0 \quad (5)$$

where ψ represents the potential. This equation (5) indicates a condition for a reflection-type boundary. Specifically, where ε_2 is sufficiently larger than ε_1 and than $\sigma\ell$, the internal electric field caused in the region Ω_2 of the dielectric member B is determined by only a fixed boundary condition applied to the region, without being affected by the dielectric member A.

The electric-field concentration-reducing effect of the invention is similar to that of a so-called field plate using a high-resistance film such as an SIPOS. However, the invention is basically different from the field plate in that the former utilizes a uniform electric field formed in the insulation film, while the latter utilizes potential distribution obtained by causing a very small amount of current to flow. To obtain the above effect of the invention, the dielectric constant of the insulation film must be sufficiently larger than that of silicon as the element material, i.e., be large enough to substantially satisfies the equation (4). Practically, it is preferable to use an insulation material having a dielectric constant five times larger than silicon. TiO_2, $BaTiO_3$, or the like is used as the insulation material. Further, it is more preferable to use an insulation film having a dielectric constant ten times larger than silicon.

Figs. 3 - 12 are cross sectional views, showing high-breakdown-voltage diodes according to 2nd - 11th embodiments of the invention. In these figures, like elements are designated by like signs, and duplication of explanation is avoided.

Fig. 3 shows a second embodiment of the invention, which has a basic structure similar to the first embodiment shown in Fig. 1, and a silicon oxide film 9 interposed between the insulation film 8 of a large dielectric constant and n-type silicon layer 1 of high resistance. Also in the second embodiment, the electric field in the insulation film 8 has uniform potential distribution when a reverse bias voltage is applied, which reduces the degree of concentration of an electric field extending into the silicon layer 1 through the oxide film 9. The thickness of the oxide film 9 is preferably less than 1 µm.

Fig. 4 shows a third embodiment of the invention, which employs insulation films 13 (13_1, 13_2, 13_3) having a large dielectric constant. The diode according to this embodiment has a dielectric isolation structure obtained, for example, by adhering a second silicon substrate 11 to the first silicon layer 1 with a silicon oxide film 10 interposed therebetween. A plurality of insulation films 13 of a large dielectric constant are formed in boundary portions between the silicon layers 1 and 10. The reason why a plurality of insulation films 13 are formed in the diode is that they are not connected to the anode and cathode electrodes 4 and 7.

In the above structure, when the n-type silicon layer 1 becomes a complete depletion layer at the time of applying a reverse bias voltage thereto, the entire voltage is applied to that portion of the depletion layer which extends between the high-concentration p-type layer 2 and high-concentration n-type layer 6. At this time, the potentials of the insulation films 13, which are in a floating state, are determined depending upon the positions thereof, and the degree of electric field in each insulation film 13 is sufficiently lower than in the ambient circumstance. Accordingly, in a bottom portion of the silicon layer 1, the potential varies in stepwise such that it

is flattened in the insulation films 13 in the horizontal direction. Thus, concentration of an electric field caused in the insulation films 13 by the influence of the side of the substrate 11 is relaxed, thereby providing high-breakdown-voltage characteristics.

Fig. 5 shows a fourth embodiment of the invention which employs an insulation film 13 formed on the over all lower surface of the n-type silicon layer 1. In this embodiment, the both opposite ends of the insulation film 13 are connected to an anode electrode 4 and a cathode electrode 7 which extend to the bottom of the element. For the same reason described in the case of Fig. 1 where the insulation film 8 is provided on the upper surface of the element, concentration of an electric field in a lower portion of the layer 1 is relaxed.

Fig. 6 shows a fifth embodiment which is a substantial combination of the structures shown in Figs. 1 and 5. In the fifth embodiment, insulation films 8 and 13 of a large dielectric constant are formed on the lower and upper surfaces of an end portion of the n-type silicon layer 1, respectively, thereby providing a diode having a higher breakdown voltage.

Fig. 7 shows a sixth embodiment which is a combination of the structures of Figs. 1 and 4. This embodiment also provides superior high-breakdown-voltage characteristics.

Fig. 8 shows a seventh embodiment, in which a low-concentration p^--type layer 15 is formed, in the upper surface of the n-type high resistance silicon layer (substrate) 1, around and in contact with a high-concentration p^+-type layer 2 selectively formed as anode element region in the upper surface of the layer 1. The diode according to this embodiment also has a high breakdown voltage, since concentration of an electric field caused in the upper surface of the high-resistance silicon layer when a reverse bias voltage is applied is relaxed.

Fig. 9 shows an eighth embodiment based on the structure of Fig. 8. This embodiment differs from the Fig. 8 embodiment only in that a p^{--}-type layer 16 having an impurity concentration lower than the low-concentration p^--type layer 15 formed in contact with the p^+-type layer 2, is formed in contact with the layer 15.

In the eighth embodiment, electric field concentration at a bottom corner of the p^+-type layer 2 can be more relaxed. As a result, a depletion layer formed in the n-type layer 1 at the time of application of a reverse bias voltage has a shape gradually decreasing in thickness from the surface and disappearing as the distance from the p^+-type layer 2 increases. Thus, the breakdown voltage is effectively enhanced as compared with the seventh embodiment.

Fig. 10 shows a ninth embodiment, which differs from the structure of Fig. 3 only in that a low-concentration p^--type layer 15 is formed, in the upper surface of the n-type high-resistance silicon layer (substrate) 1, around and in contact with the high-concentration p^+-type layer 2 as anode terminal region. The diode according to this embodiment also has a high breakdown voltage, since concentration of an electric field caused in the upper surface of the high-resistance silicon layer is relaxed when a reverse bias voltage is applied.

Fig. 11 shows a tenth embodiment, which differs from the structure of Fig. 10 in that the anode electrode 4 is formed to cover the low-concentration p^--type layer 15. The diode according to this embodiment also has a high breakdown voltage, since concentration of an electric field caused in the upper surface of the high-resistance silicon layer is relaxed when a reverse bias voltage is applied.

Fig. 12 shows an eleventh embodiment, which differs from the Fig. 11 structure in that a p^{--}-type layer 16 having an impurity concentration lower than the low-concentration p^--type layer 15 formed in contact with the p^+-type layer 2, is formed in contact with the layer 15.

In the eleventh embodiment, electric field concentration at a bottom corner of the p^+-type layer 2 is further relaxed, and a depletion layer formed in the n-type layer 1 has a shape gradually decreasing in thickness from the surface and disappearing as the distance from the p^+-type layer 2 increases. Thus, the breakdown voltage is effectively enhanced as compared with the seventh embodiment.

Though the above-described embodiments relate to pn-junction diodes, the invention is applicable also to various high-breakdown-voltage planar element such as a MOSFET, an IGBT, a bipolar transistor, a thyrister, which include a diode structure similar to that employed in the above embodiments.

Then, an embodiment will be explained in which the invention is applied to an IGBT.

Fig. 13 shows an essential part of an IGBT according to a twelfth embodiment, and Figs. 14A - 14G shows the manufacturing procedure thereof. The structure of the IGBT will be explained based on the procedure.

First, a deep p^+-type layer 36 is formed by diffusion in the upper surface of a p^--type silicon layer 31 having a p^+-type layer 30 (see Fig. 13) formed on its lower surface. Similarly, an n-type layer 32 serving as n-type base layer and an n^--type layer 33 extending around and in contact with the former are formed in that portion of the upper surface of the layer 31 which is located closer to the center than the layer 36 (Fig. 14A).

Thereafter, a thick field oxide film 38 is formed on the overall surface of the layer 31, and then selective etching is performed. Subsequently, a gate oxide film 39 is formed on an exposed portion of the silicon layer 31. (Fig. 14B)

A polycrystal silicon film 51 as gate electrode material is formed on the overall surface of the resultant structure. Subsequently, a photoresist pattern 52 is formed on the film 51, and the film 51 is selectively etched. Ions

of boron are injected into openings in the film 51. (Fig. 14C)

Then, a p-type base layer 34 is formed by performing thermal drive-in diffusion of the injected boron ions. Simultaneously, an oxide film 41 is formed on the surface of the element. (Fig. 14D)

Thereafter, a gate electrode 40 is formed by selectively etching those extra portions of the polycrystal silicon film 51 which are located on the drain side of the element, thereby forming a gate electrode 40. At this time, the oxide film 41 is removed with part thereof left, thereby exposing part of the electrode 40. Subsequently, an insulation film 42 of a large dielectric constant is provided on the resultant structure such that it extends from those portions of the field oxide film 38 which lie on the n-type base layer 32 and n^--type layer 33, to the exposed portion of the gate electrode 40. (Fig. 14E)

Thereafter, an p^+-type layer 48 and an n^+-type layer 35 serving as the drain and source of the element, respectively, are formed using the gate electrode 40 and dielectric insulation film 42 as part of a mask. Further, a p^+-type layer 37 is formed by diffusion on the side of the source so as to reduce the contact resistance. (Fig. 14F)

Then, an insulation film 43 is deposited all over the resultant structure, and contact holes are formed, followed by forming drain and source electrodes 44 and 45. The drain electrode 44 is formed such that it contacts the dielectric insulation film 42 and part of it is positioned above the gate electrode. (Fig. 14G)

In the IGBT constructed as above, when a gate circuit of a low-output impedance is connected between the gate and source, and a positive voltage is applied, a potential inclination uniform in the horizontal direction occurs in the insulation film of a large dielectric constant having both opposite ends provided with drain and gate potentials, respectively. Accordingly, electric field concentration in the element is relaxed, and local electric field concentration is prevented in the vicinity of the source junction. Further, since an electric field is forcibly formed in the insulation film 42, a depletion layer extends also from the surface of the n^--type layer 33. That is, a complete depletion layer is formed in the layer 33 even when the impurity concentration thereof is higher than in the case of the conventional element, and therefore satisfactory high-breakdown-voltage characteristics can be obtained.

Fig. 15 shows a thirteenth embodiment, in which the invention is applied to a thyrister structure. In this embodiment, a p-type layer 62 is formed in the lower surface of a high-resistance n-type silicon substrate 61. P-type layers are selectively formed in the substrate 61 from the upper and lower surfaces.

A high-concentration p^+-type layer 65 is formed in the lower surface of the substrate 61, and an electrode 66 is formed on the lower surface of the resultant structure.

A p-type layer 67 is selectively formed in that portion of the n-type substrate which is surrounded by the p-type layers 62, 63, and 64. Also, a high-concentration n^+-type layer 68 is selectively formed in the surface of the p-type layer 67, and an electrode 69 is formed on the layer 68. A high-concentration n^+-type layer 70 is selectively formed in the surface of the p-type layer 64, and an electrode 71 is formed on the layer 70. An insulator 72 having a large dielectric constant extends between the electrodes 69 and 71.

In the thirteenth embodiment, when a bias voltage of O is applied to the electrode 66 and a positive bias voltage is applied to the electrode 69, a reverse bias voltage is applied to the junction between the layers 67 and 68. Similarly, a reverse bias voltage is applied to the junctions between the n-type substrate 61 and p-type layers 62, 63, and 64. At this time, the dielectric member 72 of a large dielectric constant formed on the upper surface of the element can relax electric field concentration in the surface portion of the element, thereby obtaining a high breakdown voltage.

Claims

1. A high-breakdown-voltage semiconductor element comprising:
   a semiconductor layer (1) of a first conductivity type having a high resistance;
   a first region (3, 6) formed in the semiconductor layer and containing a highly-concentrated impurity of the first conductivity type;
   a second region (2) formed in the semiconductor layer away from the first region by a predetermined distance, and containing a highly-concentrated impurity of the second conductivity type; and
   an insulation film (8) formed adjacent to the semiconductor layer and between the first and second regions, the insulation film being made of a material having a dielectric constant larger than a material constituting the semiconductor layer.

2. The semiconductor element according to claim 1, further including a first electrode (5, 7) contacting the first region and a second electrode (4) contacting the second region, the insulation film (8) being disposed between the first and second electrodes in contact therewith.

3. The semiconductor element according to claim 1, characterized in that the insulation film (8) directly contacts the semiconductor layer (1).

4. The semiconductor element according to claim 1, characterized in that the insulation film (8) is formed on the semiconductor layer (1) with a thin film (9) interposed therebetween.

5. The semiconductor element according to claim 4, characterized in that the thin film (9) comprises an insulator.

6. The semiconductor element according to claim 2, characterized in that the insulation film (8) is formed directly on the upper surface of the semiconductor layer (1).

7. The semiconductor element according to claim 2, characterized in that the insulation film (8) is formed on the upper surface of the semiconductor layer (1) with a thin oxide film (9) interposed therebetween.

8. The semiconductor element according to claim 3, characterized in that the insulation film (13) is formed on the lower surface of the semiconductor layer (1).

9. The semiconductor element according to claim 8, characterized in that the insulation film comprises a plurality of segments (13_1, 13_2, 13_3) separate from one another and located along the semiconductor layer (1).

10. The semiconductor element according to claim 1, characterized in that the insulation film comprises insulation films (8, 13) formed on the upper and lower surfaces of the semiconductor layer (1).

11. The semiconductor element according to claim 1, further including a third region (15) formed in the semiconductor layer (1) and containing a low-concentrated impurity of the second conductivity type, the third region being formed between the first and second regions (3, 2) in contact with the second region (2).

12. The semiconductor element according to claim 1, characterized in that the insulation film (8) is formed over an end pn-junction.

13. A high-breakdown-voltage semiconductor element comprising:
a semiconductor layer (1);
a first conductivity-type region (3, 6) and a second conductivity-type region (2) which are formed in the semiconductor layer;
first and second electrodes (5, 7, 4) provided on the semiconductor layer such that they are located one on either side of a junction between the first and second conductivity-type regions; and
an insulation film (8) interposed between first and second electrodes in contact therewith, the insulation film being made of a material having a dielectric constant larger than a material constituting the semiconductor layer.

14. The semiconductor element according to claim 13, characterized in that the first and second electrodes (5, 7, 4) contact the first and second conductivity-type regions (3, 6, 2), respectively.

15. The semiconductor element according to claim 14, characterized in that the insulation film (8) is formed on the upper surface of the semiconductor layer (1) in direct contact therewith.

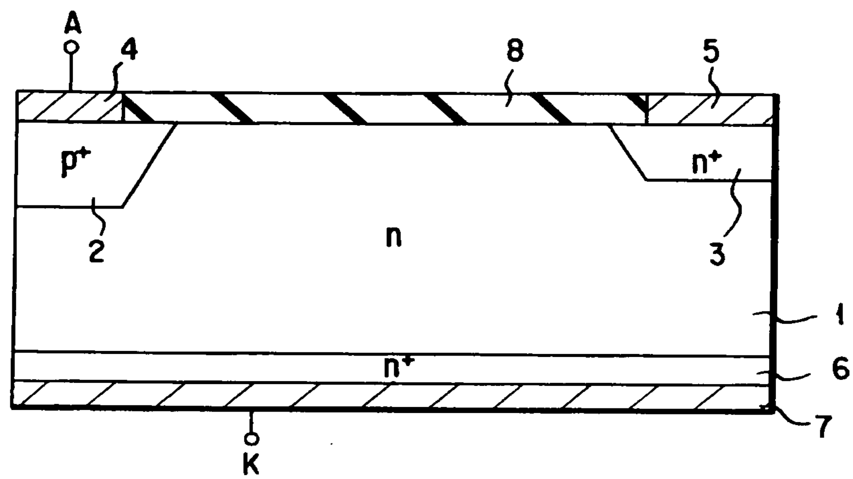
16. The semiconductor element according to claim 13, characterized in that the insulation film (8) is formed on the upper surface of the semiconductor layer (1) with a thin film (9) interposed therebetween.

17. The semiconductor element according to claim 13, characterized in that the insulation film (8) is formed on the lower surface of the semiconductor layer (1).

18. The semiconductor element according to claim 13, characterized in that the insulation film comprises insulation films (8, 13) formed on the upper and lower surfaces of the semiconductor layer (1).

19. The semiconductor element according to claim 16, characterized in that the semiconductor element is a MOSFET, wherein the first electrode is a gate electrode (40), and the second electrode is a source/drain electrode (44).

20. The semiconductor element according to claim 13, characterized in that the semiconductor element is a thyrister, wherein the first electrode is a cathode electrode (66, 71), and the second electrode is an anode electrode (69).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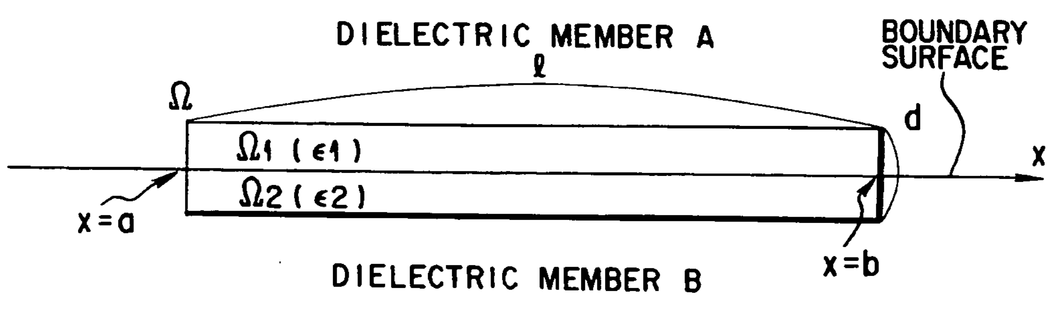
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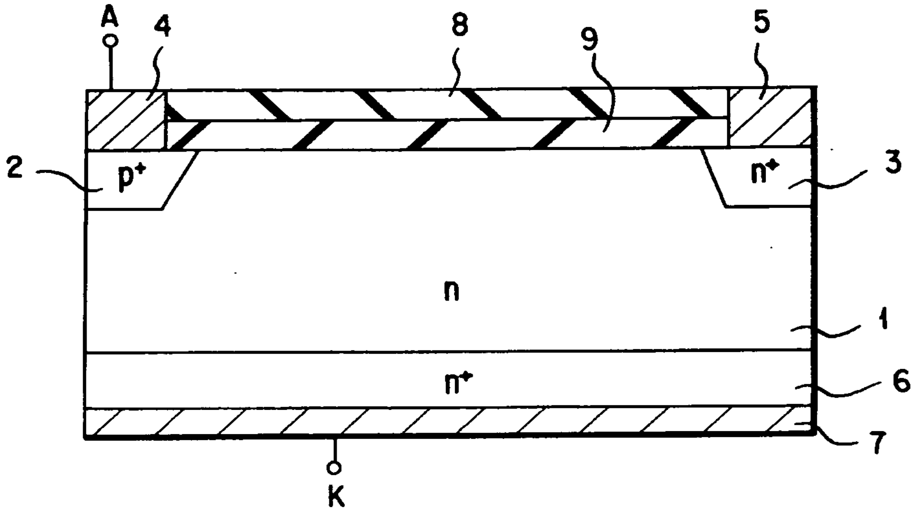
DIELECTRIC MEMBER B

F I G. 2



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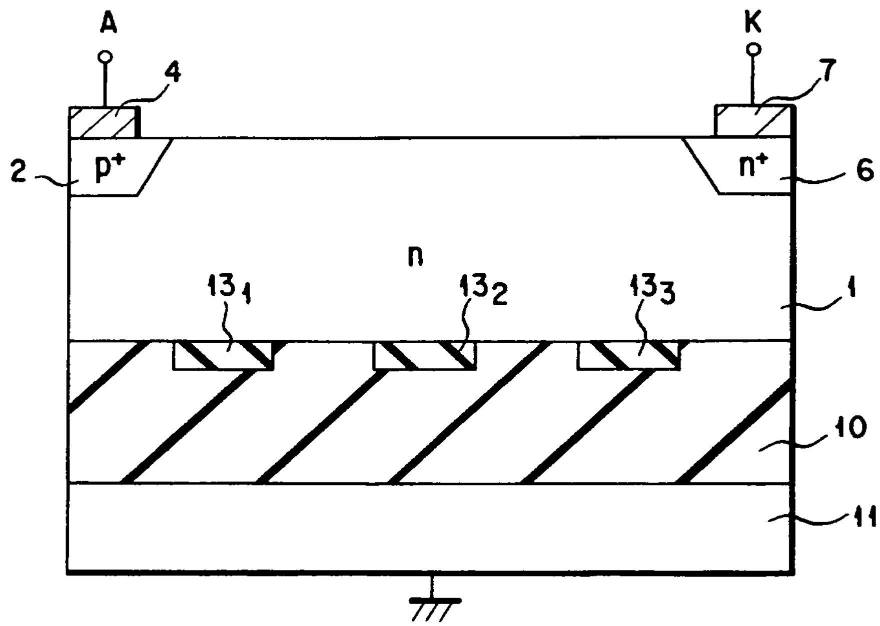

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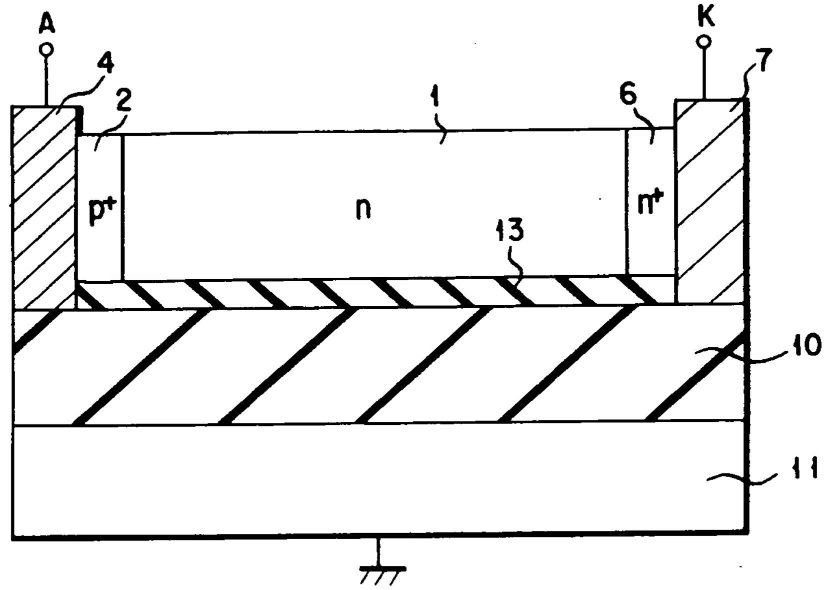

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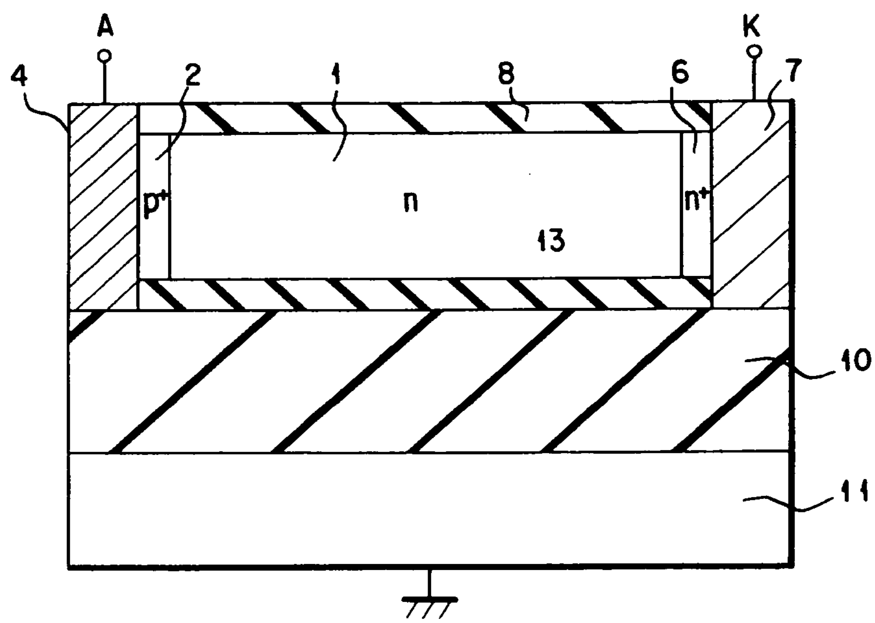

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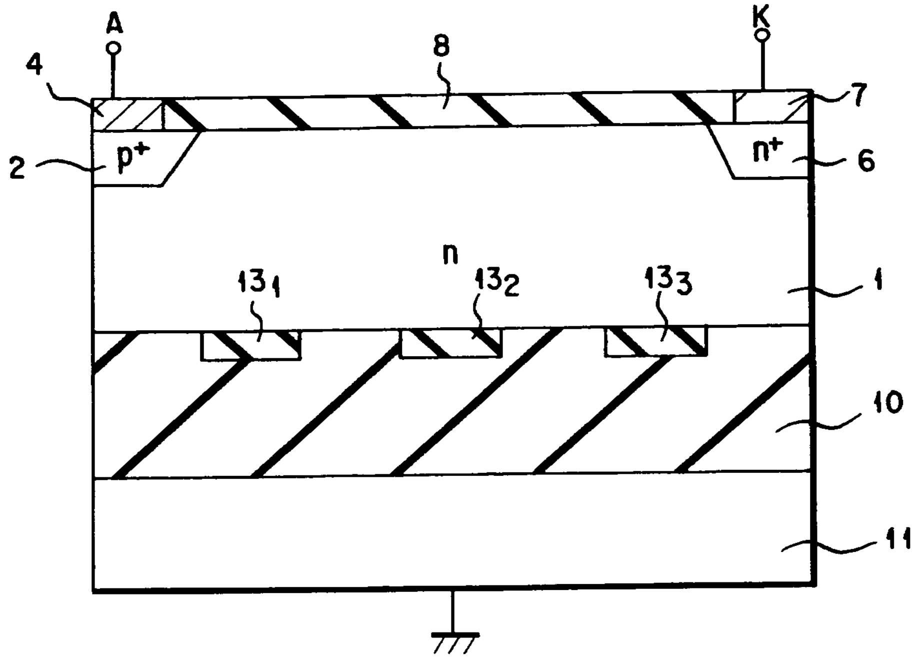

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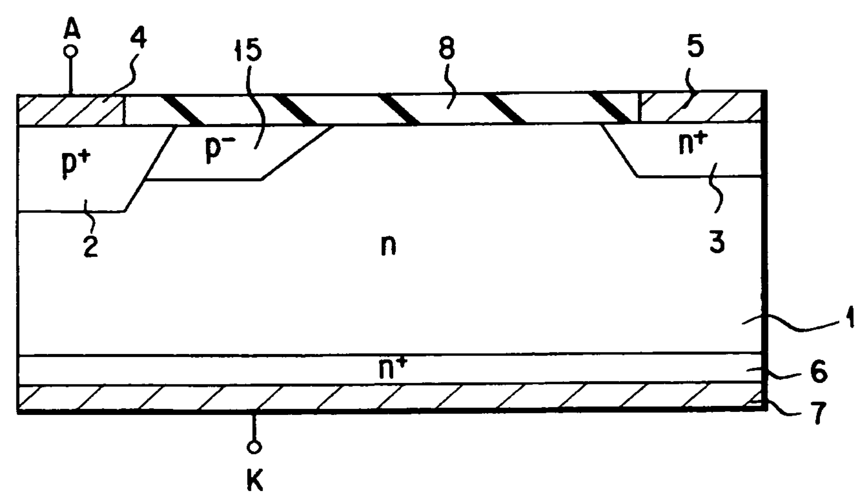

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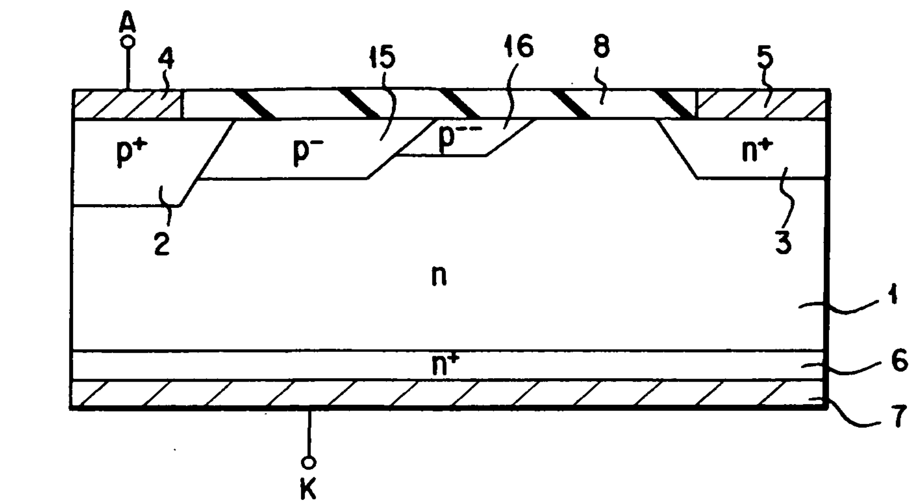

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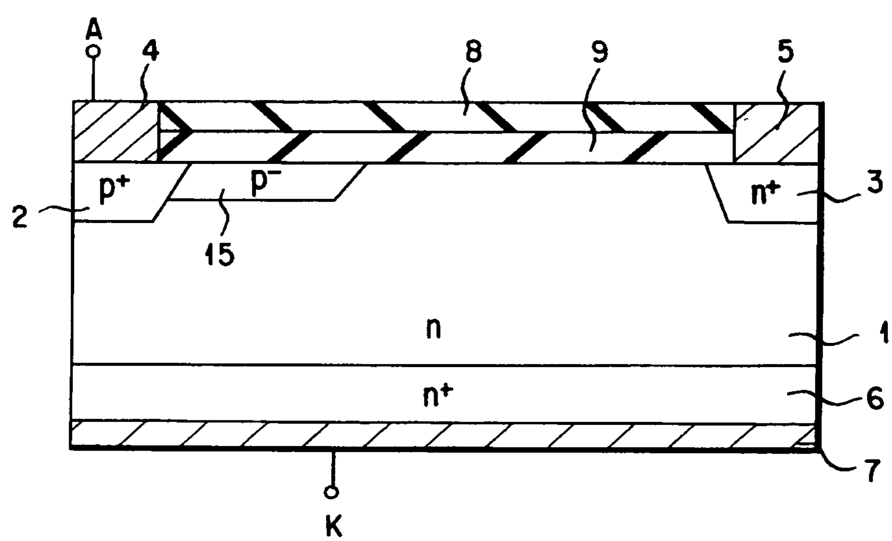

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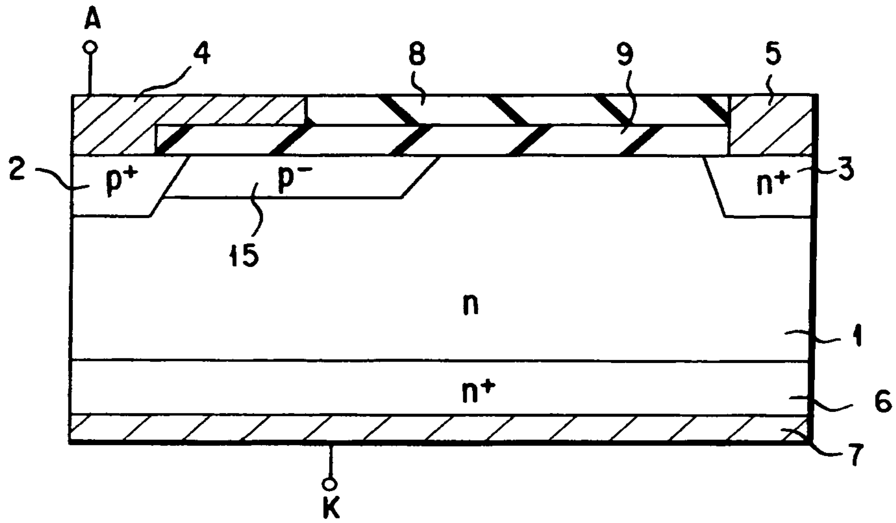
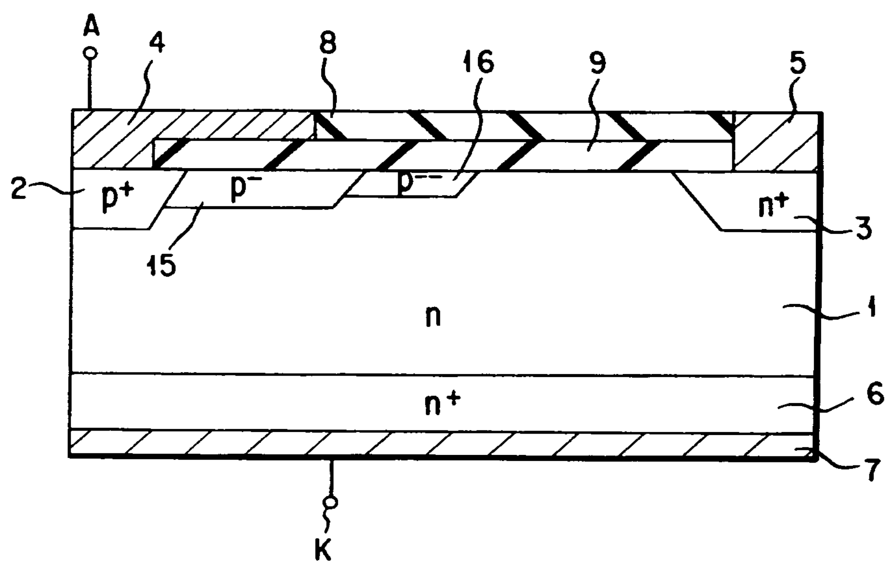


F I G. 11



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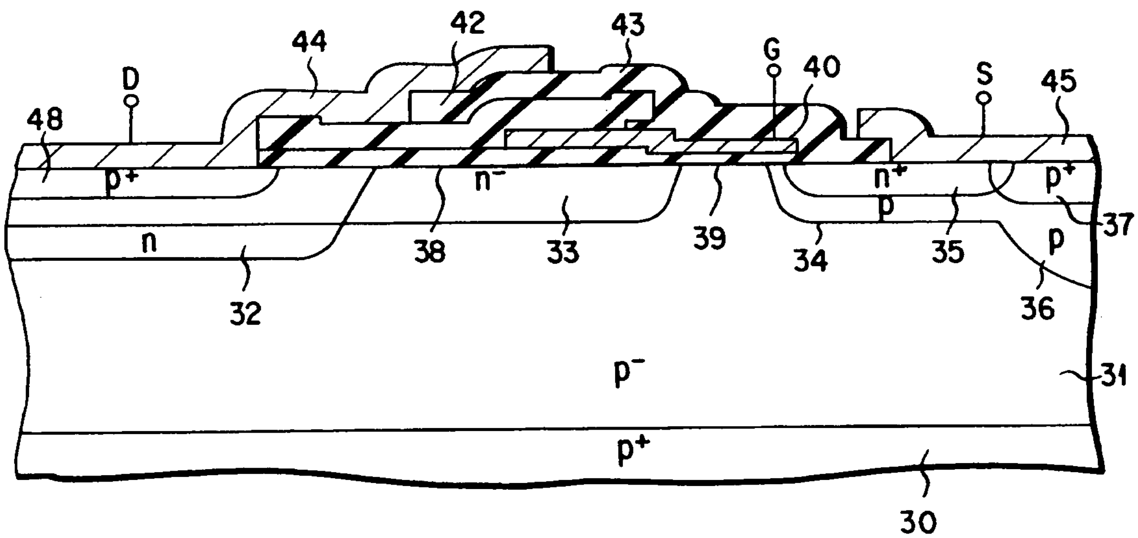

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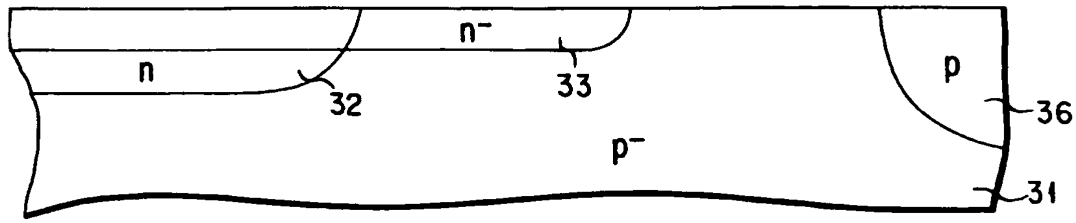

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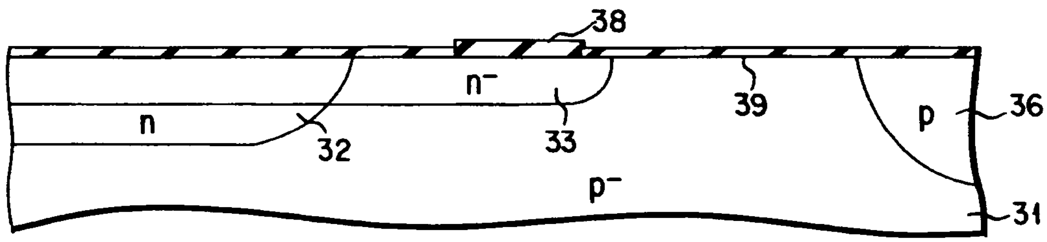

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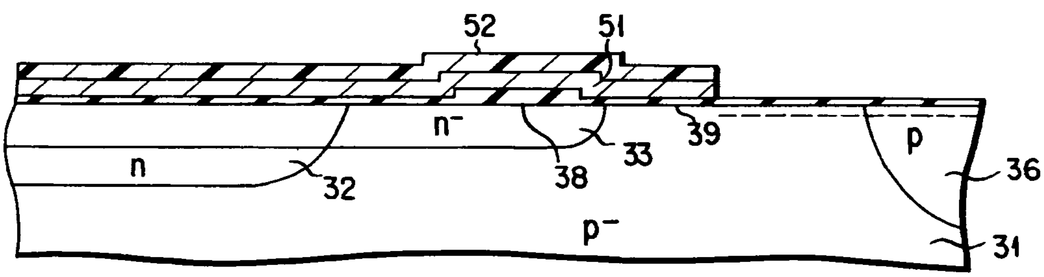

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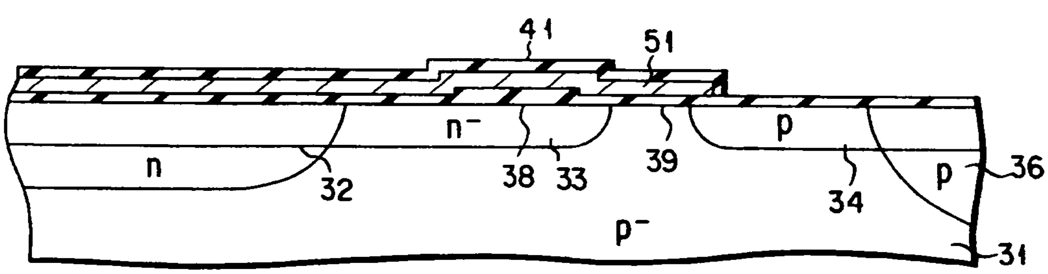

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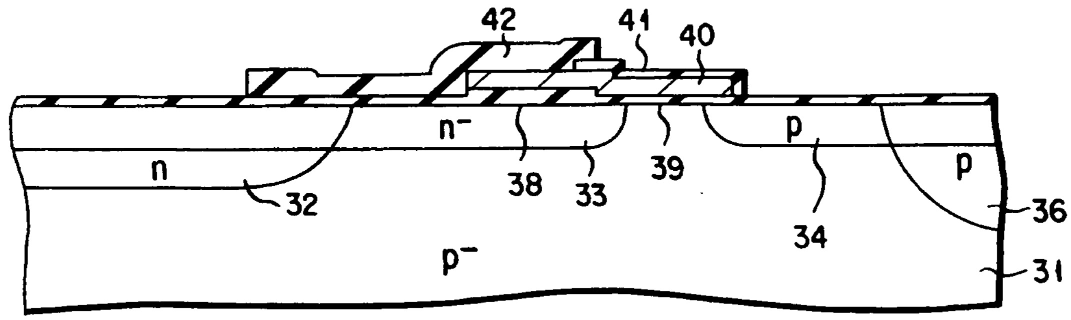

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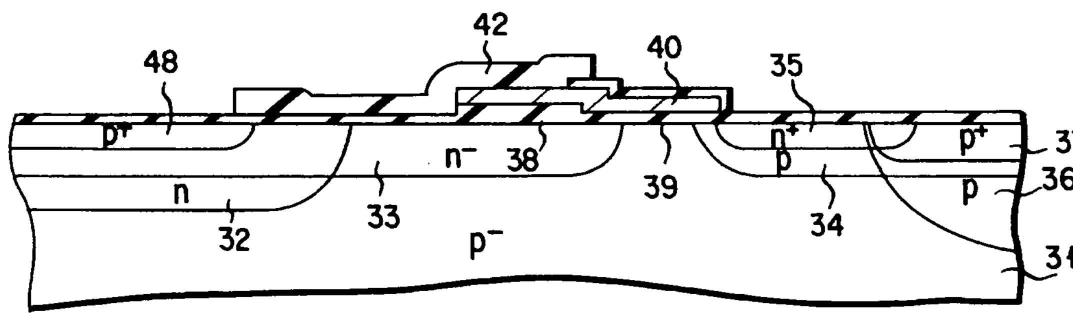

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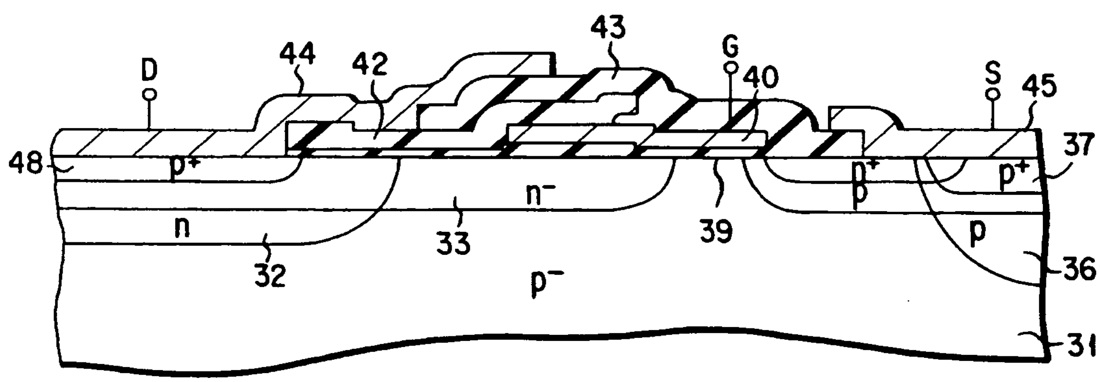

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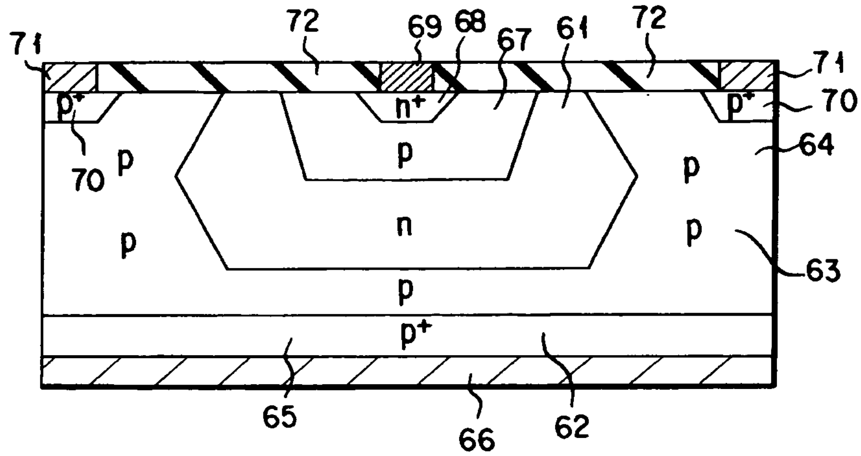
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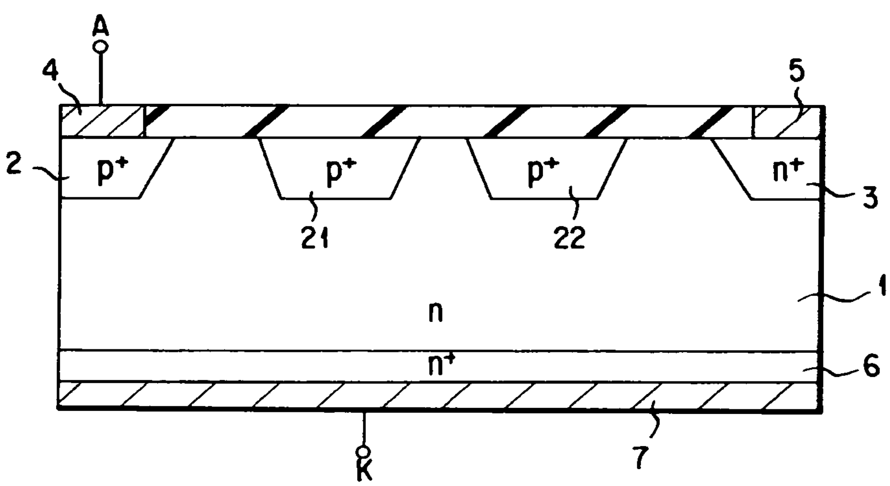
65
66
62

F I G. 15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p+
p+
n+
3
21
22
n
1
n+
6
K
7

F I G. 16